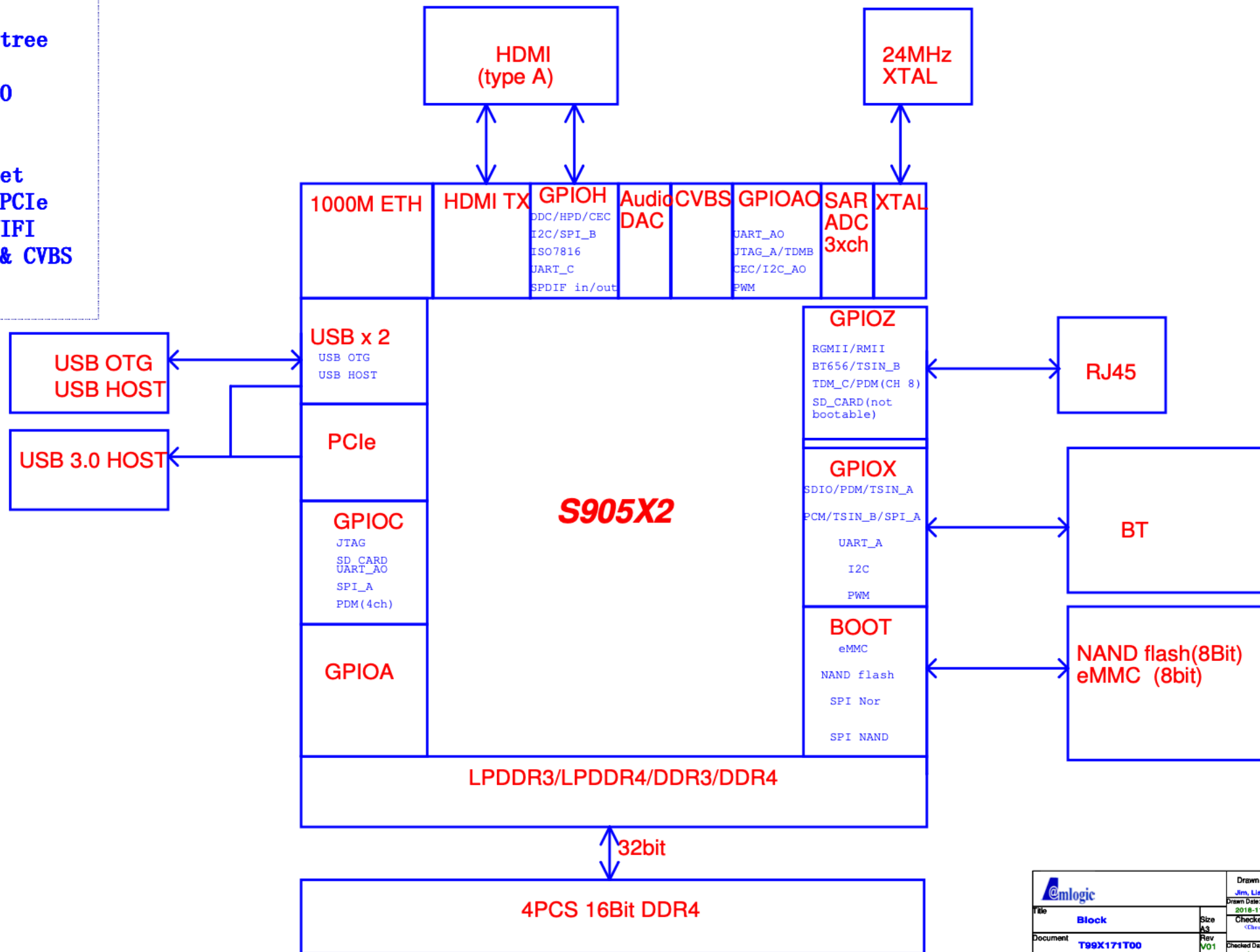


Page Index
 00- Block
 00- Power tree
 01- Power
 02- CPU I/O
 03- DDR4
 04- Flash
 05- Ethernet
 06- USB & PCIe
 07- SDIO WIFI
 08- Audio & CVBS
 09- HDMI

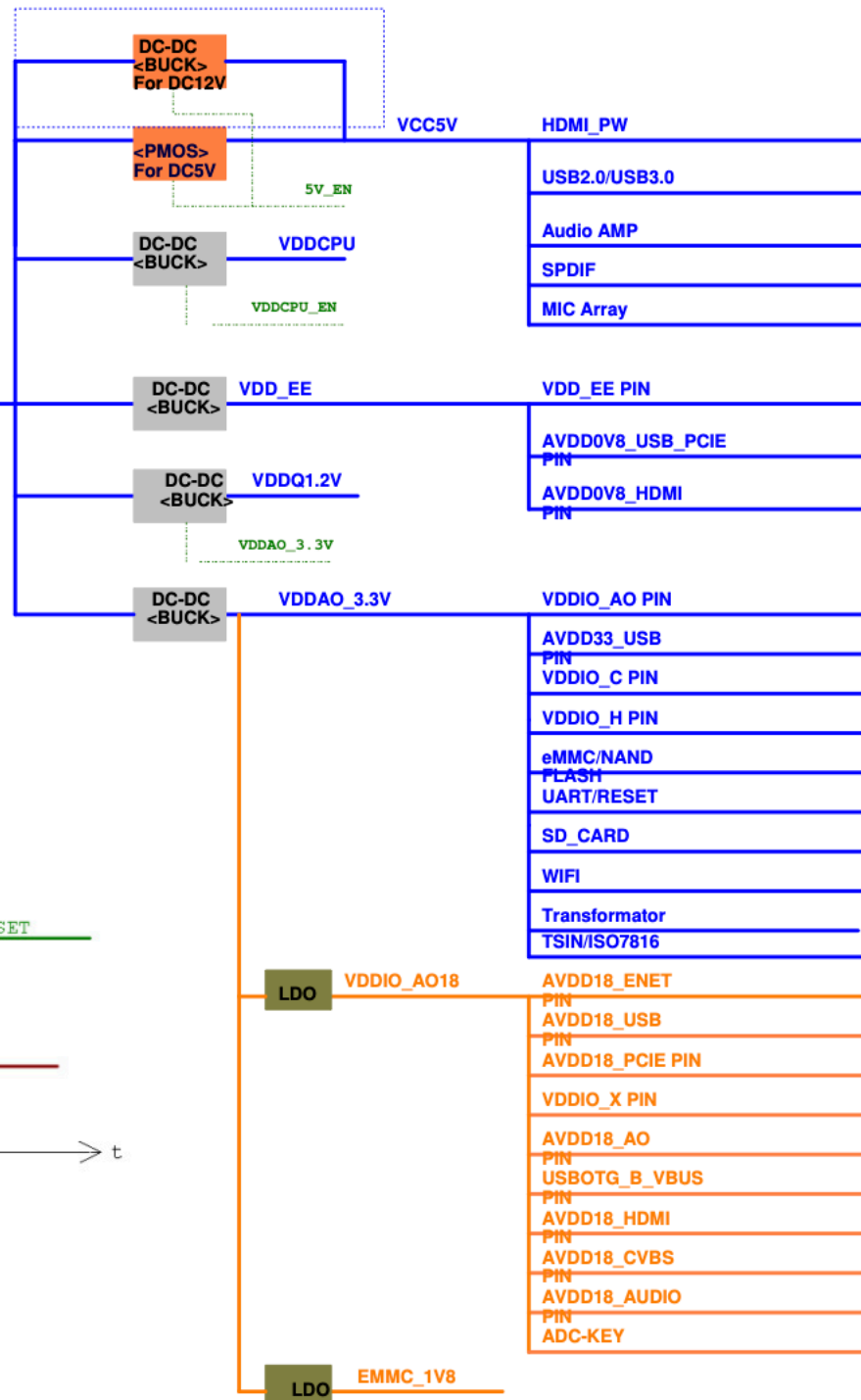
S905X2 REF BOARD DIAGRAM



Power Tree

Option:
12V@1A

Default:
5V@2A

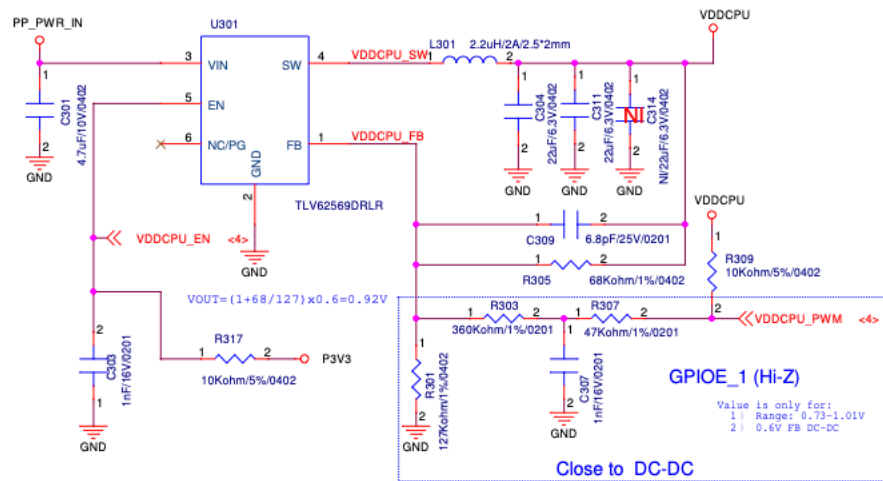


Example power on sequence:



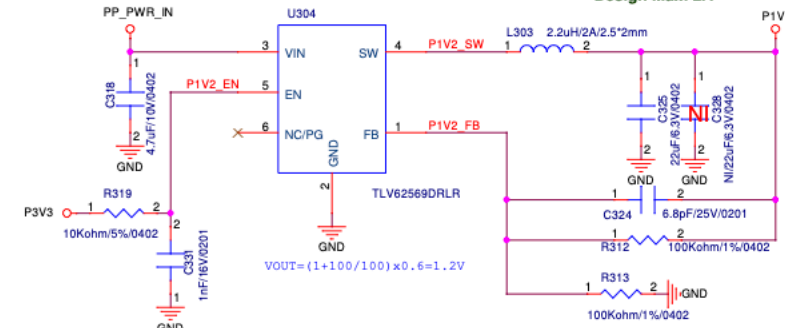
PP_PWR_IN to VDDCPU

Design Max: 2A



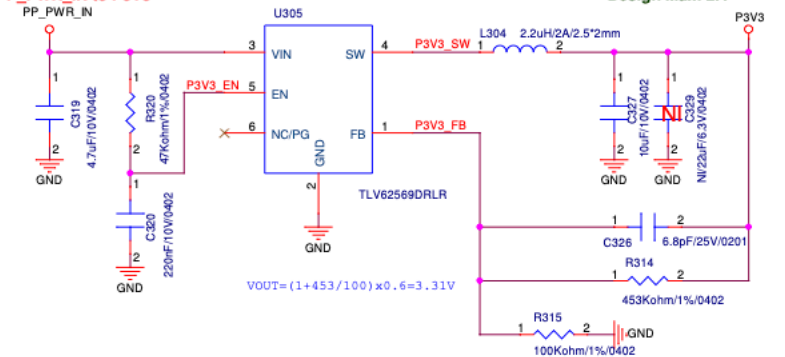
PP_PWR_IN to P1V2

Design Max: 2A



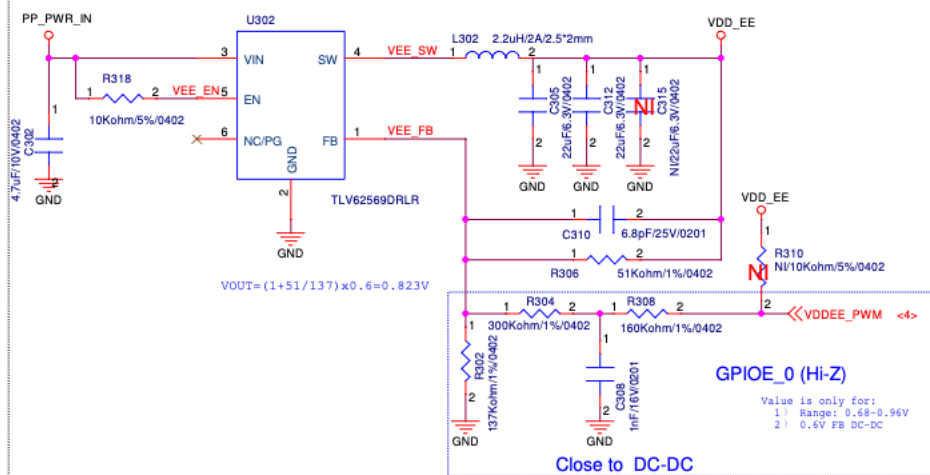
PP_PWR_IN to P3V3

Design Max: 2A



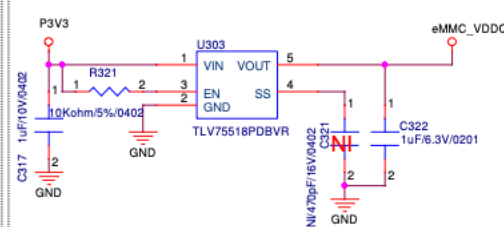
PP_PWR_IN to VDD_EE

Design Max: 2A



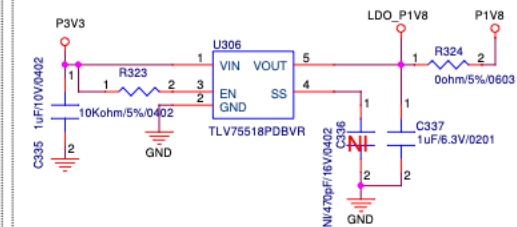
P3V3 to eMMC_VDDQ

Design Max: 500mA

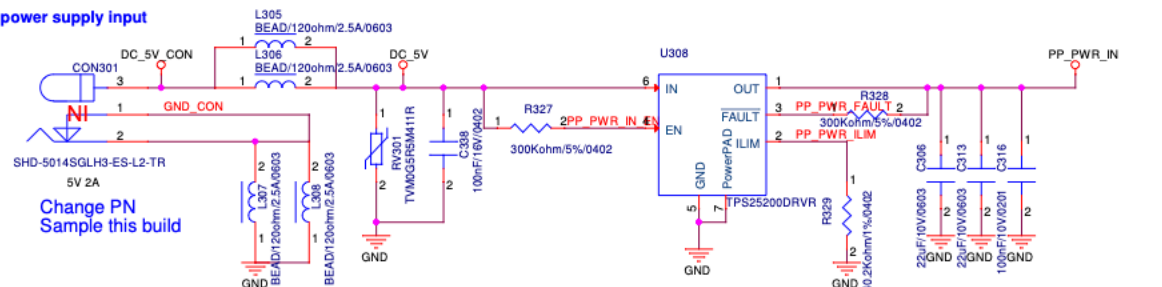


P3V3 to P1V8

Design Max: 500mA

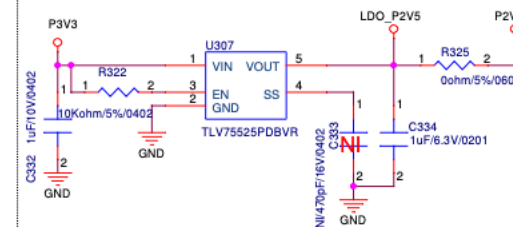


DC power supply input



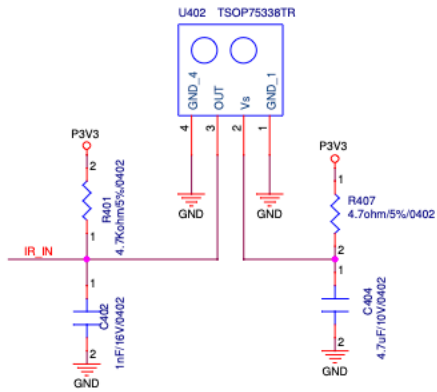
P3V3 to P2V5

Design Max: 500mA

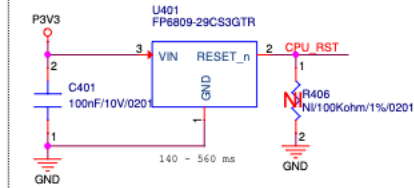


		Drawn by: Jin Liang
File Power		Drawn Date: 2018-11-20
Document T99X171T00		Checked by: V01
Date: Wednesday, March 27, 2019		Checked Date: checked date
Sheet 3 of 15		

Remote control receiver

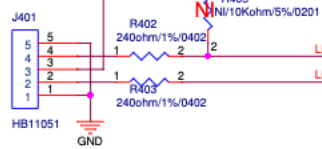


CPU RESET

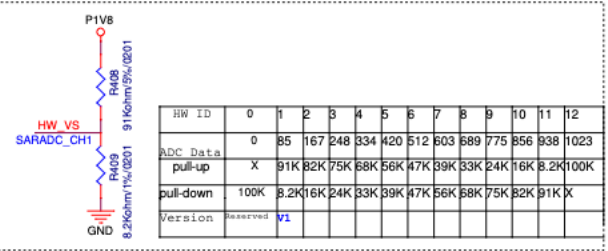
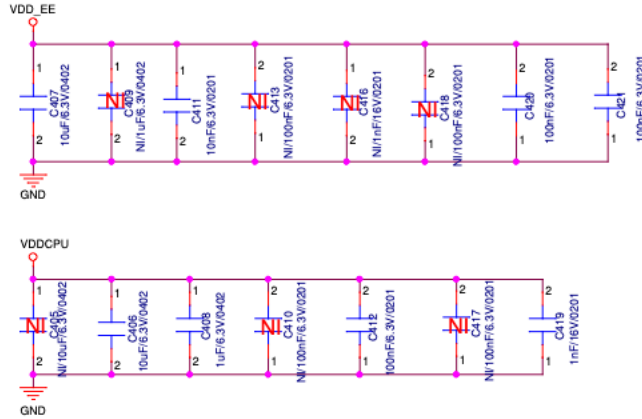
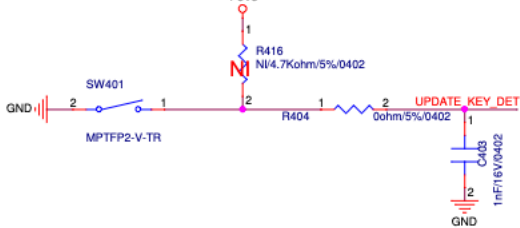


For Linux Debug

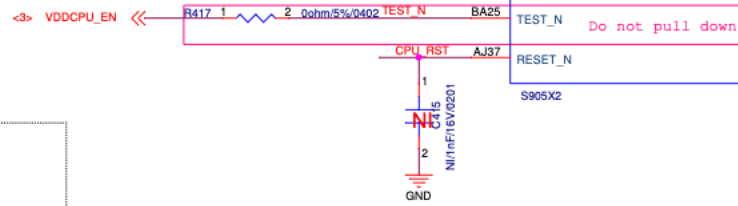
mark signal name on PCB



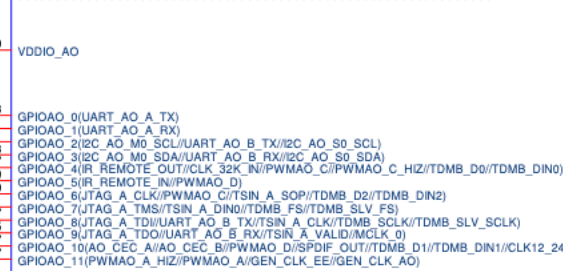
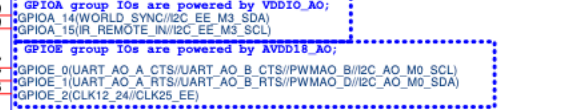
Update button



MASTER



LIB VER: 2018-01-05



RTC layout notes:
close to CPU, keep XIN/XOUT short,
Do not break GND path

		Drawn by: Jim Liang	
Title CPU I/O		Drawn Date: 2018-11-20	
Document T99X171T00		Checked by: iCheck27	
Date: Tuesday, May 07, 2019		Checked Date: checked date	
Sheet 4 of 15		Size Custom	

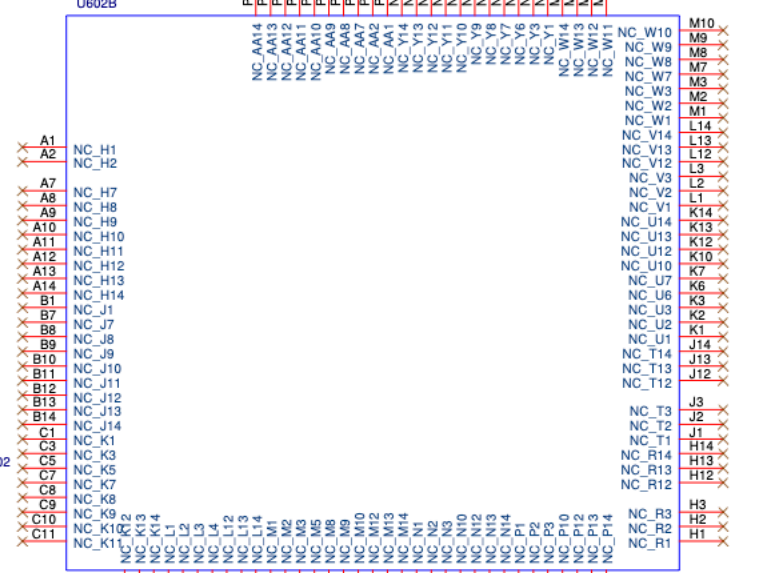
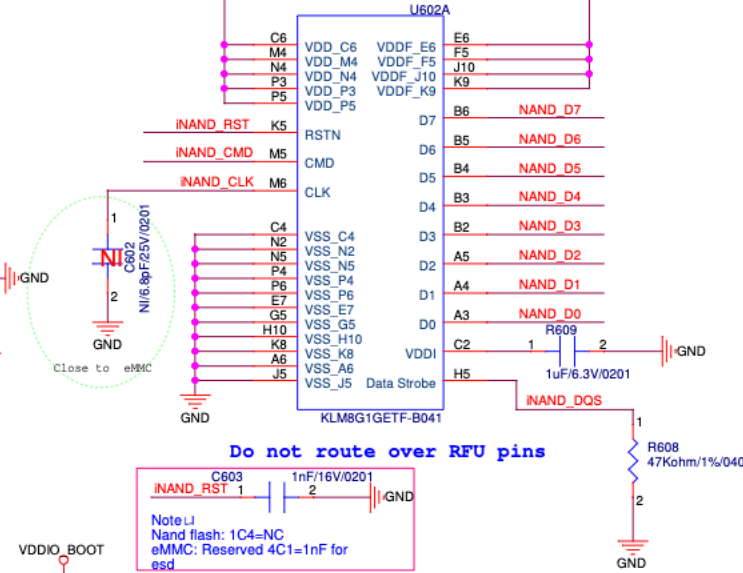
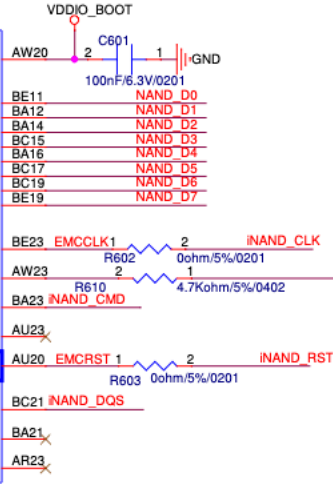
eMMC/iNAND

LIB VER: 2018-01-05

VDDIO_BOOT

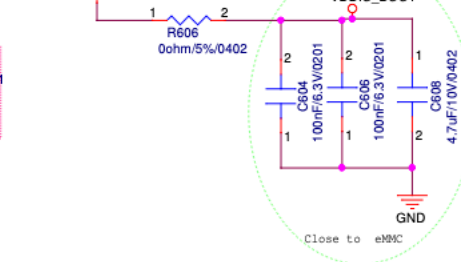
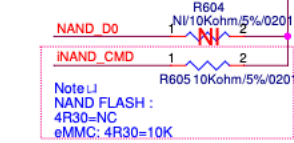
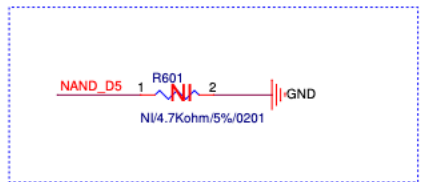
BOOT_0(EMMC_D0)
BOOT_1(EMMC_D1)
BOOT_2(EMMC_D2)
BOOT_3(EMMC_D3/NOR_HOLD)
BOOT_4(EMMC_D4/NOR_D)
BOOT_5(EMMC_D5/NOR_Q)
BOOT_6(EMMC_D6/NOR_C)
BOOT_7(EMMC_D7/NOR_WP)
BOOT_8(EMMC_CLK/NAND_WEN_CLK)
BOOT_9(NAND_ALE)
BOOT_10(EMMC_CMD/NAND_CLE)
BOOT_11(NAND_CEO)
eMMC reset GIPO BOOT_12(NAND_REN_WR)
BOOT_13(EMMC_NAND_DQS)
BOOT_14(NAND_RB0/NOR_CS)
BOOT_15(NAND_CEI)

S905X2



Power ON Config

BOOT_5[NAND_D5]: 0= USB Boot First



U1G

LIB VER: 2018-01-05

ENET_TXP
ENET_TXN

ENET_RXP
ENET_RXN

ENET_ATP

ENET_EXTRES

DVSS_3

AVDD18_ENET

U29

GND

P1V8

L33

VDDIO_Z

AV39

C701

1uF/6.3V/0201

GND

GPIOZ_0(ETH_MDIO//ISO7816_CLK//BT656_A_VS//I2C_EE_M0_SDA)
GPIOZ_1(ETH_MDC//ISO7816_DATA//BT656_A_HS//I2C_EE_M0_SCL)

GPIOZ_2(ETH_RGMII_RX_CLK//TSIN_B_VALID/TDMC_D0/TDMC_DIN0/PDM_DIN0/SDCARD_D0)
GPIOZ_3(ETH_RX_DV//TSIN_B_SOP/BT656_A_CLK/TDMC_D1/TDMC_DIN1/PDM_DIN1/SDCARD_D1)
GPIOZ_4(ETH_RXD0//TSIN_B_DIN0/BT656_A_DIN0/TDMC_D2/TDMC_DIN2/PDM_DIN2/SDCARD_D2)
GPIOZ_5(ETH_RXD1//TSIN_B_CLK/BT656_A_DIN1/TDMC_D3/TDMC_DIN3/PDM_DIN3/SDCARD_D3)
GPIOZ_6(ETH_RXD2_RGMII//TSIN_B_FAIL/BT656_A_DIN2/TDMC_FS/TDMC_SLV_FS/PDM_DCLK/SDCARD_CLK)
GPIOZ_7(ETH_RXD3_RGMII//TSIN_B_DIN1/BT656_A_DIN3/TDMC_SCLK/TDMC_SLV_SCLK//I2C_EE_M0_SDA/SDCARD_CMD)

CARD port on GPIOZ is not bootable

GPIOZ_8(ETH_RGMII_TX_CLK//TSIN_B_DIN2/BT656_A_DIN4/MCLK_1/I2C_EE_M0_SCL)
GPIOZ_9(ETH_TXEN//TSIN_B_DIN3/BT656_A_DIN5)
GPIOZ_10(ETH_TXD0//TSIN_B_DIN4/BT656_A_DIN6)
GPIOZ_11(ETH_TXD1//TSIN_B_DIN5/BT656_A_DIN7)
GPIOZ_12(ETH_TXD2_RGMII//TSIN_B_DIN6)
GPIOZ_13(ETH_TXD3_RGMII//TSIN_B_DIN7/GEN_CLK_EE)
GPIOZ_14(OD3.3V)(ETH_LINK_LED//I2C_EE_M2_SDA)
GPIOZ_15(OD3.3V)(ETH_ACT_LED//I2C_EE_M2_SCL)

S905X2

C39

A39

C41

A41

L26

J26

U29

L33

AV39

C701

1uF/6.3V/0201

GND

AR37

RGMII MDIO

R701

1

2

0ohm/5%/0402

MDIO <8>

AR39

RGMII MDC

R702

1

2

0ohm/5%/0402

MDC <8>

BC43

RGMII RX CLK

R703

1

2

22ohm/5%/0402

RXCLK_PHYAD1 <8>

BE45

RGMII RXDV

R704

1

2

22ohm/5%/0402

RXCTL_PHYAD2 <8>

AW45

RGMII RXD0

R705

1

2

0ohm/5%/0201

RXD0_RXDLY <8>

AY41

RGMII RXD1

R706

1

2

0ohm/5%/0201

RXD1_TXDLY <8>

BA43

RGMII RXD2

R707

1

2

0ohm/5%/0201

RXD2_PLLOFF <8>

BA45

RGMII RXD3

R708

1

2

0ohm/5%/0201

RXD3_PHYAD0 <8>

AV41

RGMII TX CLK

R709

1

2

0ohm/5%/0402

TXCLK <8>

AU43

RGMII TXEN

R710

1

2

0ohm/5%/0402

TXEN <8>

AT41

RGMII TXD0

R711

1

2

0ohm/5%/0201

TXD0 <8>

AM37

RGMII TXD1

R712

1

2

0ohm/5%/0201

TXD1 <8>

AM39

RGMII TXD2

R713

1

2

0ohm/5%/0201

TXD2 <8>

AM35

RGMII TXD3

R714

1

2

0ohm/5%/0201

TXD3 <8>

AR45

RGMII INT

R715

1

2

22ohm/5%/0402

INTB_PMEB <8>

AR43

RGMII RST_N

R716

1

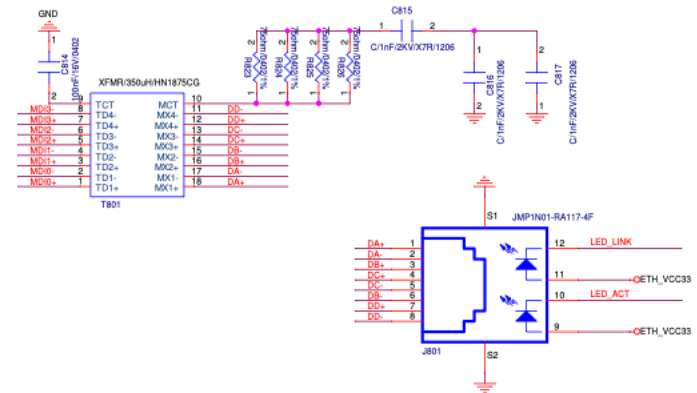
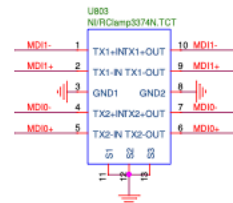
2

22ohm/5%/0402

PHY_RST <8>

Close to PHY

		Drawn by: Jim, Liang	
Title Ethernet		Drawn Date: 2018-11-20	
Document T99X171T00		Checked by: V01	
Date: Wednesday, March 27, 2019		Checked Date: checked date	
Sheet 7		of 15	



PHY_XTAL_IN 1 2 PHY_XTAL_OUT

R001 330ohm/5%/V0402

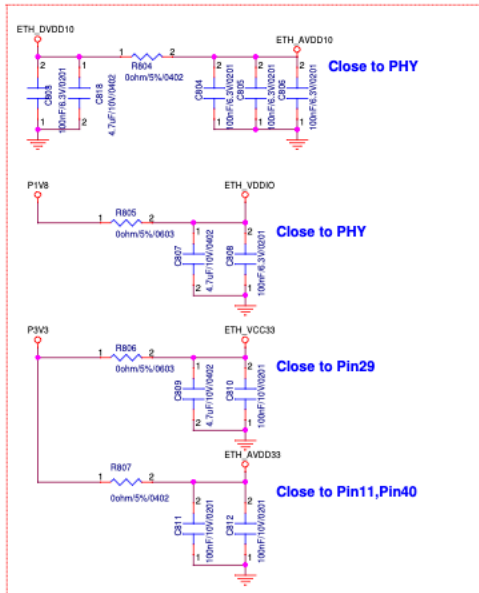
R002 330ohm/5%/V0402

YB01 25MHz

C001 18pF/5%/V0402

C002 18pF/5%/V0402

XTAL/25MHz/7ppm/12pF



The diagram shows two digital signals, PHY_RST and INTB_PMEB, over time. Both signals are active-low, indicated by a bubble on the input pin. They are connected to a 4.7kOhm resistor and a 5V/VDD2 supply. The signals are shown to be high (inactive) for most of the duration, with a brief low pulse (active) for PHY_RST. The timing is labeled with RST08 and RST09, indicating the reset duration. The signals are also connected to ETH_VCC33 and ETH_VCC33.

Use external P1V8

Pull up: Disable

Pull low: Enable

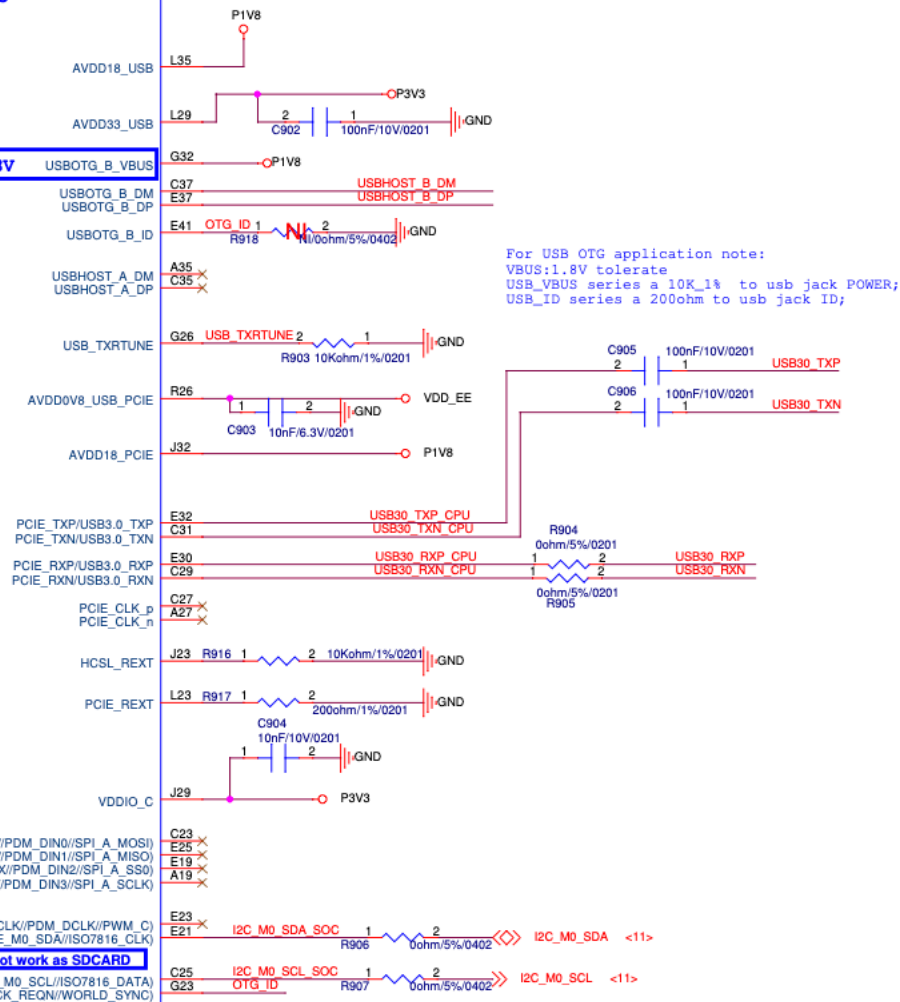
Pull up: 2ns delay
Pull low: No delay

3'b001(default)

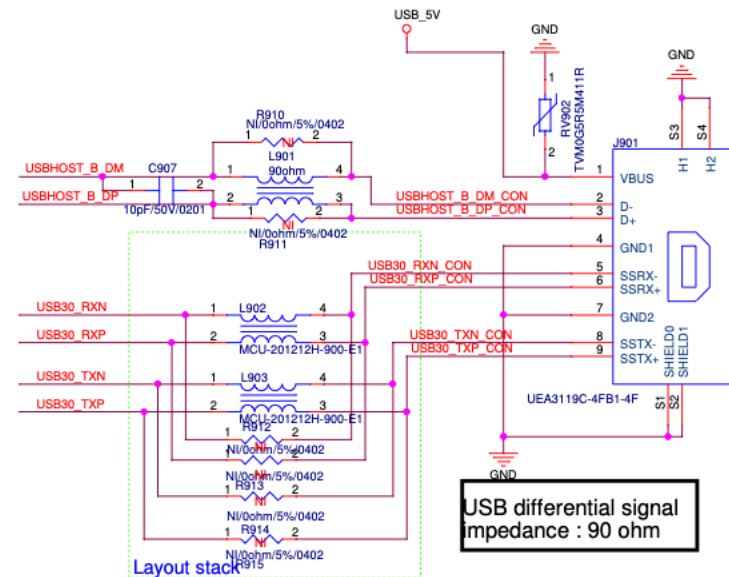
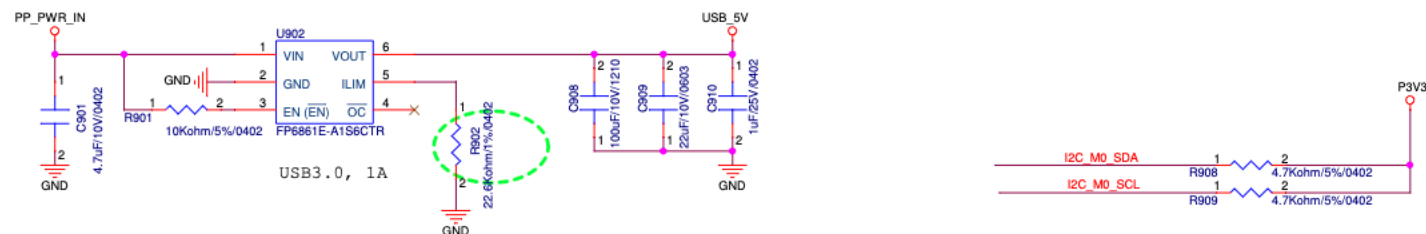
U1E

LIB VER: 2018-01-05

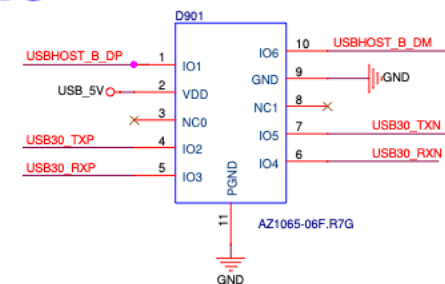
Tolerance 1.8V



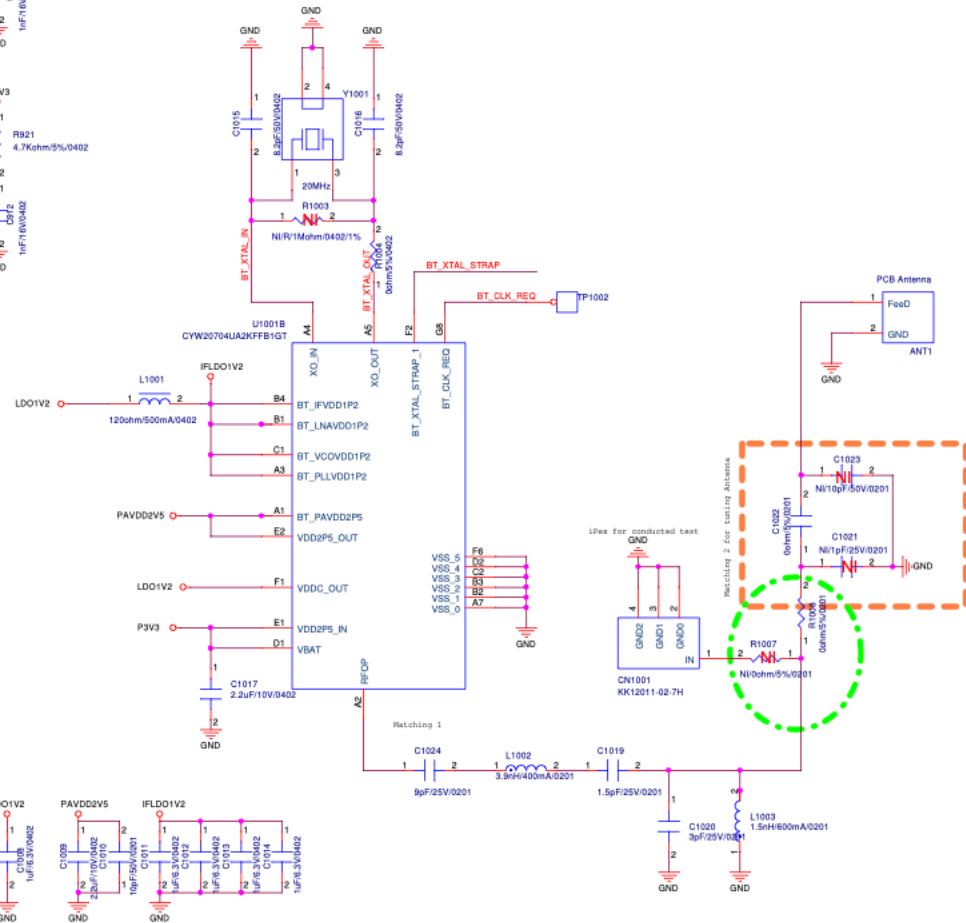
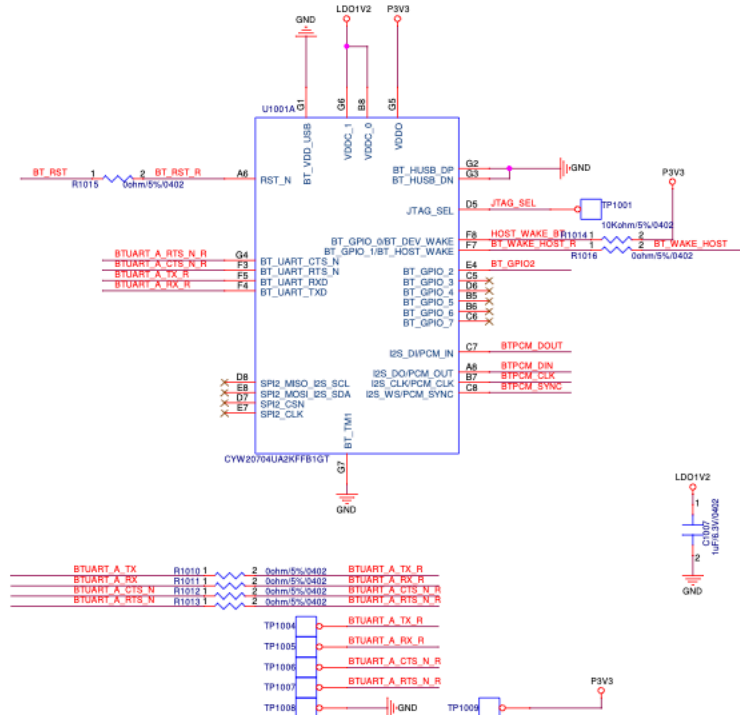
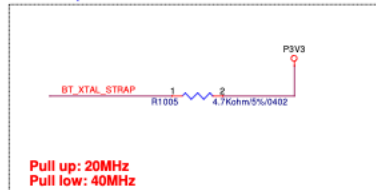
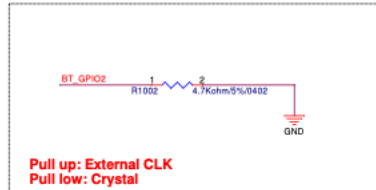
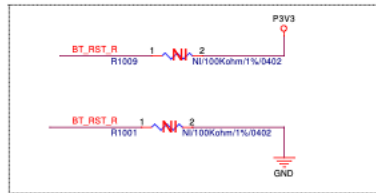
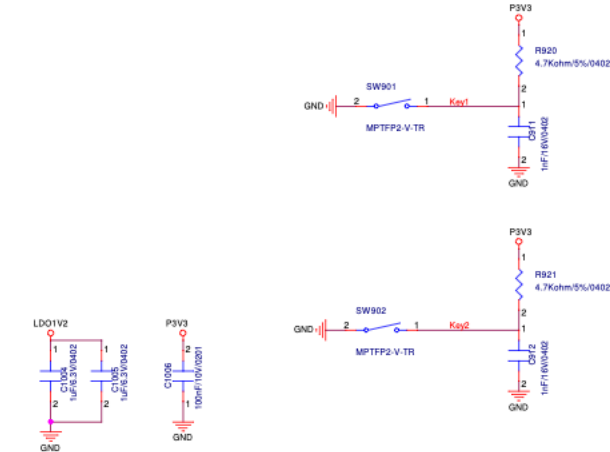
S905X2



ESD

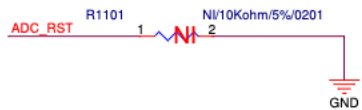


		Drawn by: Jim Liang	
Title USB & PCIe		Drawn Date: 2018-11-20	
Document T99X171T00		Checked by: (Checked)	
Date: Wednesday, March 27, 2019		Check Date: checked date	
Sheet 9 of 15		Size Custom Rev V01	

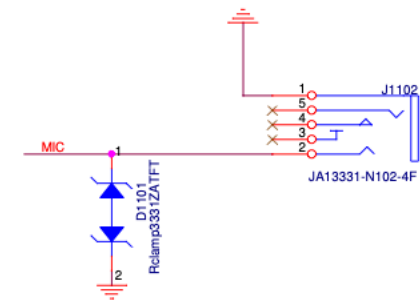
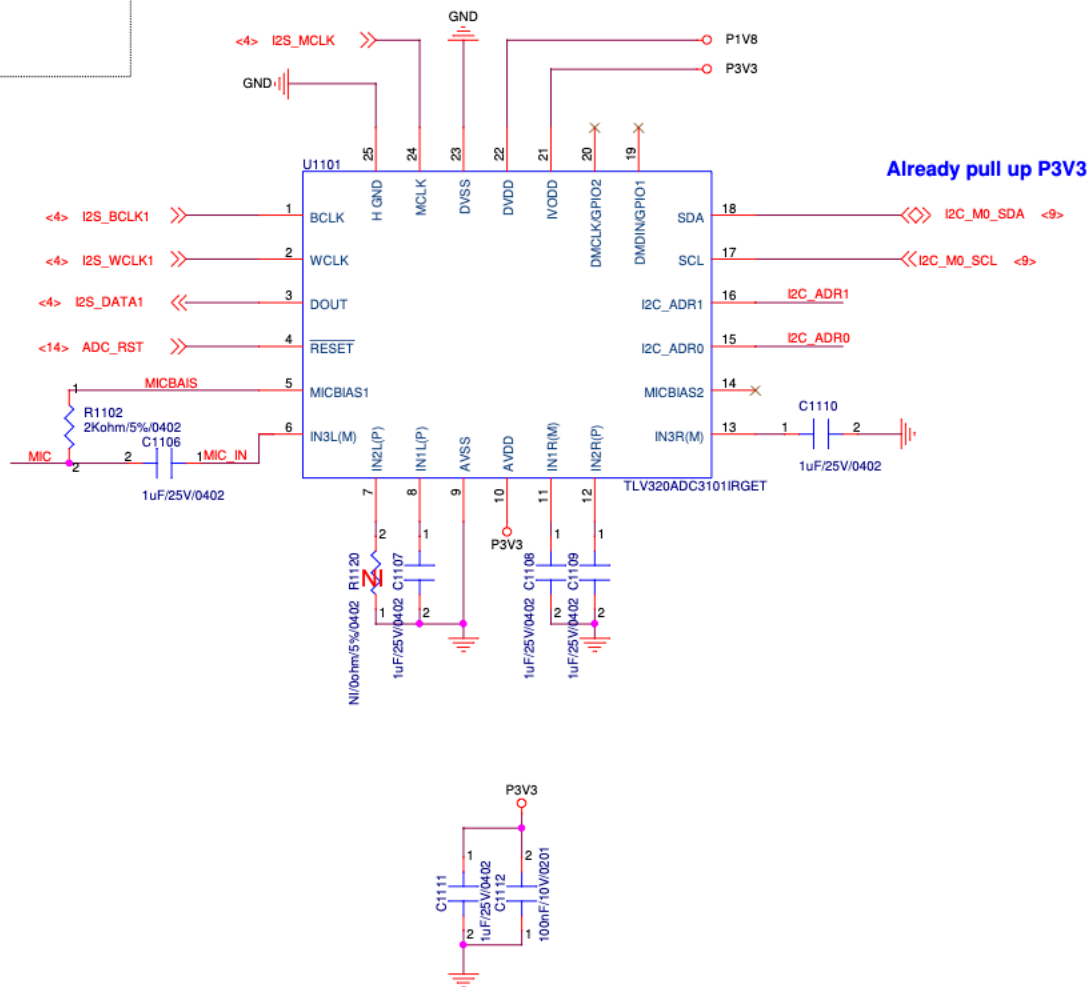


ADC RESET

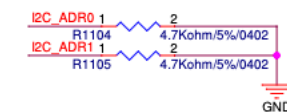
RST>10ns



SLAVE

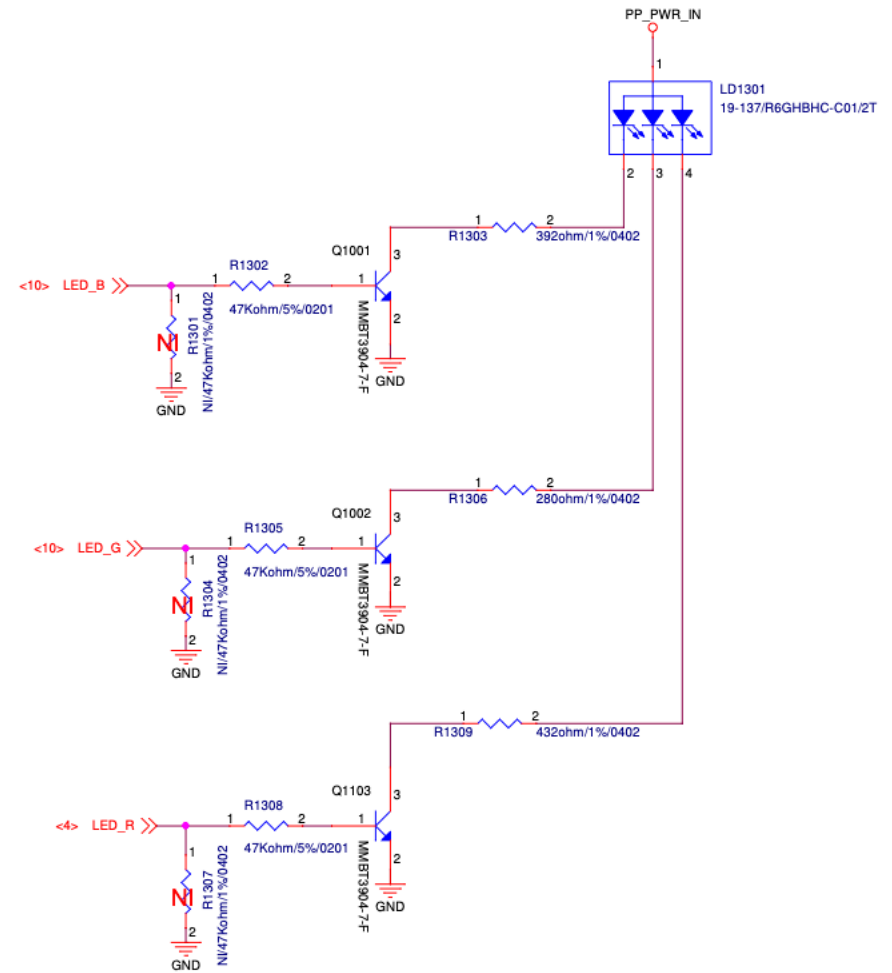
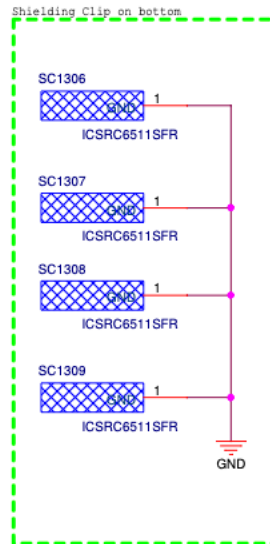
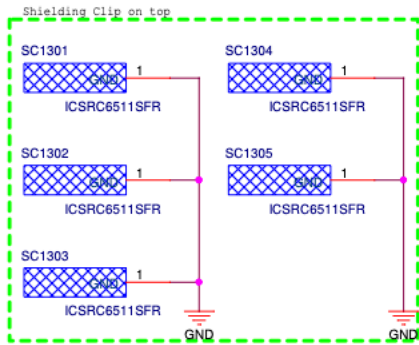
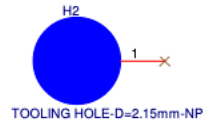
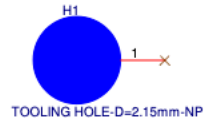


ADDRESS: 0x30



		Drawn by: Jim, Liang	
Title ADC		Drawn Date: 2018-11-20	
Document T99X171T00		Checked by: [Signature]	
Date: Wednesday, March 27, 2019		Checked Date: checked date	
Sheet 11 of 15		Rev V01	

		Drawn by: Jim, Liang	
Title DSP		Size B	Drawn Date: 2018-11-20
Document T99X171T00		Rev V01	Checked by: Checked
Date: Wednesday, March 27, 2019		checked Date: checked date	
Sheet		12 of 15	



		Drawn by: Jim, Liang	
Title LED/CLIP		Size B	Drawn Date: 2018-11-20
Document T99X171T00		Rev V01	Checked by: checked date
Date: Tuesday, July 02, 2024		Sheet 13	of 15

LIB VER: 2018-01-05

VDDIO_H

GPIOH_0 (OD5V) (HDMITX_SDA/I2C_EE_M3_SDA)
GPIOH_1 (OD5V) (HDMITX_SCL/I2C_EE_M3_SCL)
GPIOH_2 (OD5V) (HDMITX_HPD_IN/I2C_EE_M1_SDA)
GPIOH_3 (OD5V) (I2C_EE_M1_SCL/AO_CEC_A/AO_CEC_B)

GPIOH_4 (SPDIF_OUT/UART_EE_C_RTS/SPI_B_MOSI)
GPIOH_5 (SPDIF_IN/UART_EE_C_CTS/SPI_B_MISO/PWM_F/TDMB_D3/TDMB_DIN3)

GPIOH_6 (ISO7816_CLK/UART_EE_C_RX/SPI_B_SS/I2C_EE_M1_SDA)
GPIOH_7 (ISO7816_DATA/UART_EE_C_TX/SPI_B_SCLK/I2C_EE_M1_SCL)
GPIOH_8 (OD5V)

AVDD0V8_HDMI

AVDD18_HDMI

HDMI_CEXT

HDMI_REXT

DVSS_2

HDMITX_CK_P

HDMITX_CK_N

HDMITX_0P

HDMITX_0N

HDMITX_1P

HDMITX_1N

HDMITX_2P

HDMITX_2N

AVDD18_CVBS

CVBS_COMP

CVBS_VREF

CVBS_RSET

CVBS_IOUT

AVSS_CVBS

AVDD18_AUDIO

LOLP

LOLN

LORP

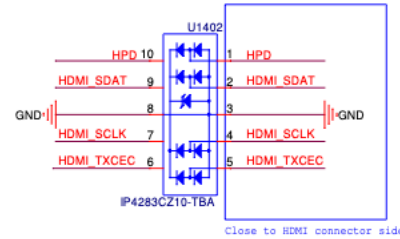
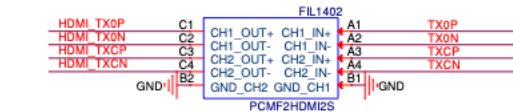
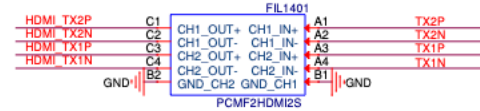
LORN

REFP

VMID

AVSS_AUDIO

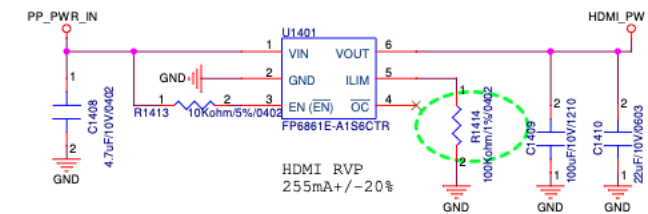
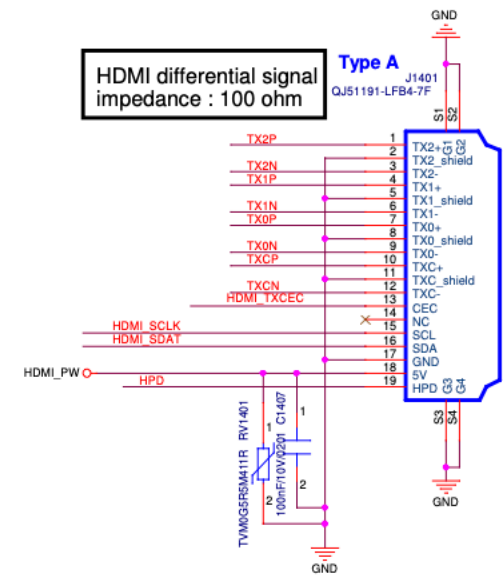
HDMI output



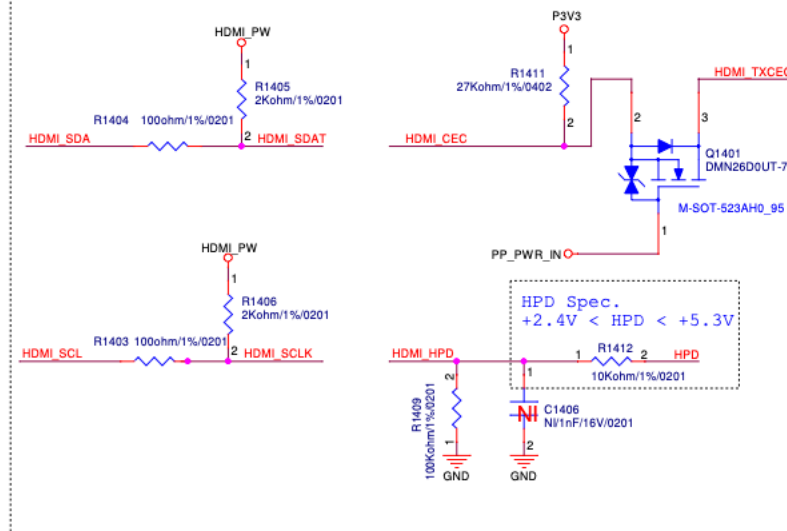
HDMI differential signal impedance : 100 ohm

Type A

QJ51191-LFB4-7F

HDMI (power) Spec.
+4.8V < PVDD5 < +5.3V

9Q2 防倒灌電路, 9R2/9R1 分壓電路不可刪除



Version	Change List	Date
001	First version of T99X171T00	2018/11/01

Version	Change List	Date
002	First version of T99X171T00	2019/03/15

- Page 3.
- 1. OVP and OCP: Change D301 and F301 to TPS25200 solution
 - 2. P1V8 LDO ripple: Change U303 and 306 from 027.01421.005 to JSTLV75518PDBV
 - 3. P2V5 LDO ripple: Change U303 and 306 from 027.01437.005 to JSTLV75525PDBV
- Page 4.
- 4. Slove I2S overshoot and undershoot:Change R412, R413, R414, R415 from 0ohm to 49.9ohm
 - 5. Support wake on BT: Change Net BT_WAKE_HOST fom GPIOX_18 to GPIOAO_2
- Page 7.
- 6. No use for reserve EMI: Delete C702 22p
- Page 8.
- 7. Xtal 25M: Change R802 from 0ohm to 330ohm
 - 8. For phy bringup: add C818 4.7u
 - 9. RGMII TXC/RXC Delay Config: Tx 2ns dealy, pop R814 and R815 nopop
Rx no dealy, pop R813 and R812 nopop
- Page 9.
- 10. USB OTG_ID control pin change to open drain pin: Change OUG_ID from GPIOC_1 to GPIOC_7
- Page 10.
- 11. Xtal 20M: Change C1015 and C1016 from 18p to 8.2p
 - 12. LED (B) change default pull up pin: change LED_B from GPIOAO_11 to GPIO_X5
 - 13. LED (G) change default pull up pin: change LED_G from GPIO_X6 to GPIO_X7
- Page 11.
- 14. ADC change AGND ro GND: Delete R1103, R1106, R1107, R1108, C1113
- Page 14.
- 15. Change HDMI I2C pull up from PP_PWR_IN to HDMI_PW